Design of Fully-Static Low-Power CVSL CMOS 128-Bit Shift Register

Walter Gordy, Josh Kotobi, and Miguel Gallegos

***Abstract*—The design proposed is a 128-bit shift register, created from CVSL CMOS technology. The shift register is designed and simulated using t-spice to optimize area, speed, and robustness. The shift register proposed will be used in a 128x128 pixel CMOS camera fabricated in 0.6μm technology. The layout was done with L-Edit.**

I. Introduction

THE project will consist of two phases. In the first phase, the schematic of the project was dicussed and the functionality was verified using SPICE simulations. In this report, we discuss the layout of the shift register on silicon, the extracted simulation, and a test plan to verify the chip after manufacturing.

II. Solution Methodology

The shift register is composed of 19 transistor CVSL CMOS flip-flops. The flip flops were designed to fit in an area of 17.7μm by 65μm. Each flip-flop has connections on each side for D, DB, Q, QB, RESET, and CLK. This allows us to connect each flip-flop flop side by side so that each connection is made automatically when we use an array.

Our proposed flip-flop is composed of a high-speed dynamic differential flip-flop, first proposed by Yuan and Swensson in 1997. By adding a minimum inverter into their second stage DSTC2 p-latch and two minimum n-transistors into the DSTC2 p-latch and DSTC1 n-latch we can create a fully static differential flip-flop with reset.

To make the DSTC2 p-latch static, we only need to prevent a low-output from floating to high and not necessarily to prevent a high-output from floating to low. If the inputs to the DSTC2 p-latch do not change, the above condition will be satisfied inherently since the high-input will pull-down the low-output always. However, when the inputs are flipped during high clock phase, the low-output loses the pull-down capability and might float to high. The SSTC2 p-latch can prevent this from occurring. Since the original high-output is pulled down by the new coming high-input, the common node will be forced down and the inverter will give a high output to the two extra n-transistors to pull all other internal nodes down firmly. Only when the clock goes low, the common node is charged to high (the inverter gives a low output to turn off the two extra n-transistors) and the latch returns to normal.

Since the phase I report, no major behavior modifications have been made. The only major changes were to decrease the transistors sizes from 8λ to 5λ. This allowed us to reduce the leakage current and reduce the size of the layout. This was nessesary to make room for the inverter chains we needed to drive signals within the chip and drive signals outside of the chip.

Our shift-register design includes 128 flip-flops to drive the pixel selection and two additional flip-flops for pulse generation and row clock generation. The pulse generation flip-flop is located at the beginning of the register and is connected to the first-bit flip-flop by cross connecting the inputs and outputs. When the reset signal occurs, this puts the pulse flip-flop into a low state, and after the first clock the flip-flop states in a high state. This one transistion propagates as a pulse through the shift-register. When the pulse reaches the end of the chain, it is carried to the row clock where the row gets shifted one bit. The same scheme occurs with the row shift-register. Reset signals are needed to restart the column and row signals. Reset is low active.

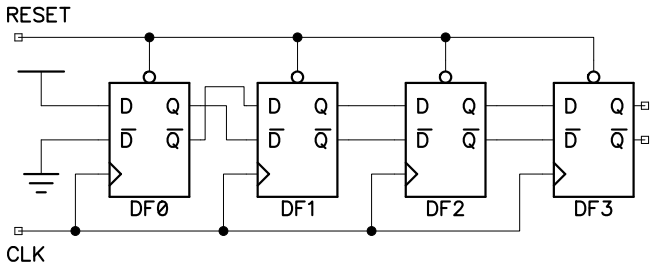

Fig. 1. Flip-flop chain showing the initialization flip-flop and the first three flip-flops of the shift register.

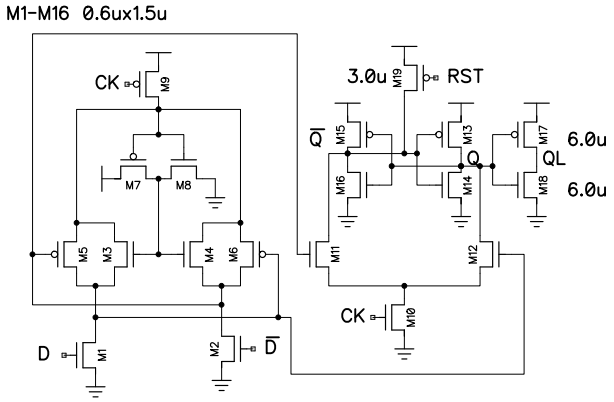

Fig. 2. Transistor Schematic of flip-flop.

W. Gordy, J Kotobi, and M Gallegos are with the Department of Electrical Engineering, University of New Mexico, Albuquerque, NM 87106.

III. Simulation and Extraction

The design was verified to run correctly using the extracted spice file from sinlge and connected flip-flops. Functionality of each type of extraction was verified and compared against the original spice file for the design. The behavior of the design was the same. We also measued other parameters of our flip-flop. The setup and hold times were measured to be approximately 825ps and 1450ps respectively. This numbers are slightly different from the spice file we ran previously since this simulation takes into account many more parameters. The setup and hold times were measured using Q and QB since our flip-flop is differential.

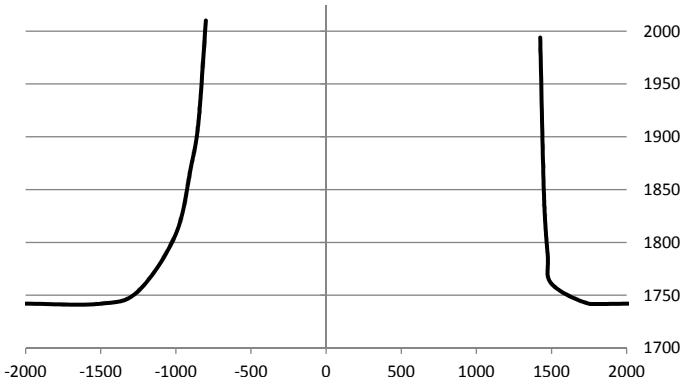

Fig. 3. Setup and Hold Times with extracted transistor capacitance. Axis are picoseconds

The rise time and fall times were measured using the extracted spice model.The rise time under normal capacitive load of 1.3pF is less than 6ns (approximately 5.8ns), and the fall time is less than 3ns (2.78ns). This puts our design well in a safe area operation since we will clocking our design with a 200ns clock maximum (5Mhz).

We ran additional performace tests to measure the minimum and maximum clock frequencies, and to verify that the design would work under all possible test conditions. The design is capable of fully static operation, and has a verified maximum clock frequency of 5Mhz, although we believe the maximum clock could be much higher, we didn't test above 5Mhz as it was outside the scope of the design.

We compared out schematic against LVS and DRC, both required tests passed 100%. The appendix shows screen shots for verification. The DRC was also run against the whole design to verify that all routing within the design was correct, this was also error free.

IV. Testing Strategy

Our testing strategy is two part, Since our flip-flop design was fairly compact, we have room to place additional testing transistors. We have the ends of row and column shift-registers output to pads. This will allow the end user to recieve feedback that the transistor register has complete its task and is ready to be reset to the beginning again.

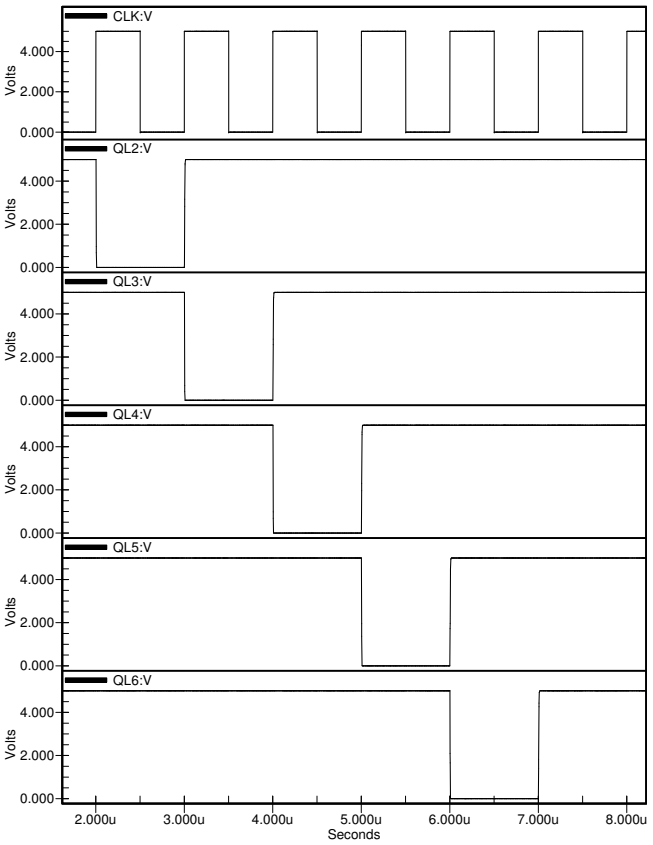

Fig. 4. Functionality of flip-flop at 1Mhz, showing standard operation with a load capacitor of 1.3pF.

In addition, our design allows for us to place more layout outside of the shift-register for testing. This will allow us to test more than just the camera. We can gain additional insight into the functionality of the flip-flop cell without having to guess. There are two flip-flops that stand alone in the layout. The first flip-flop has three buffered outputs that can each drive a 20pF load with a maximum rise/fall time of 10ns. This should all for proper testing of the flip-flop for maximum performance. The second flip flop is not buffered and will drive the pads directly. This flip flop will be slower to drive the pads, but should allow for more accurate testing. We also place a single buffer inverter for testing. The input and output signals are tied to pads. This should also allow us to verify every aspect of our design.

V. Conclusion

The results of the flip-flop concludes with a very robust, small area, low power design. The flip-flop tests well under all specified conditions, and fits in the area required. This flip-flop was chosen as the result of weeks of testing and was picked out of eight different flip-flop designs we tested. Our design allowed us to add additional functionality to the design, which we feel is a great benefit to the project since this will allow the chip to be used for two purposes.

Luckily our design had space at the bottom to place

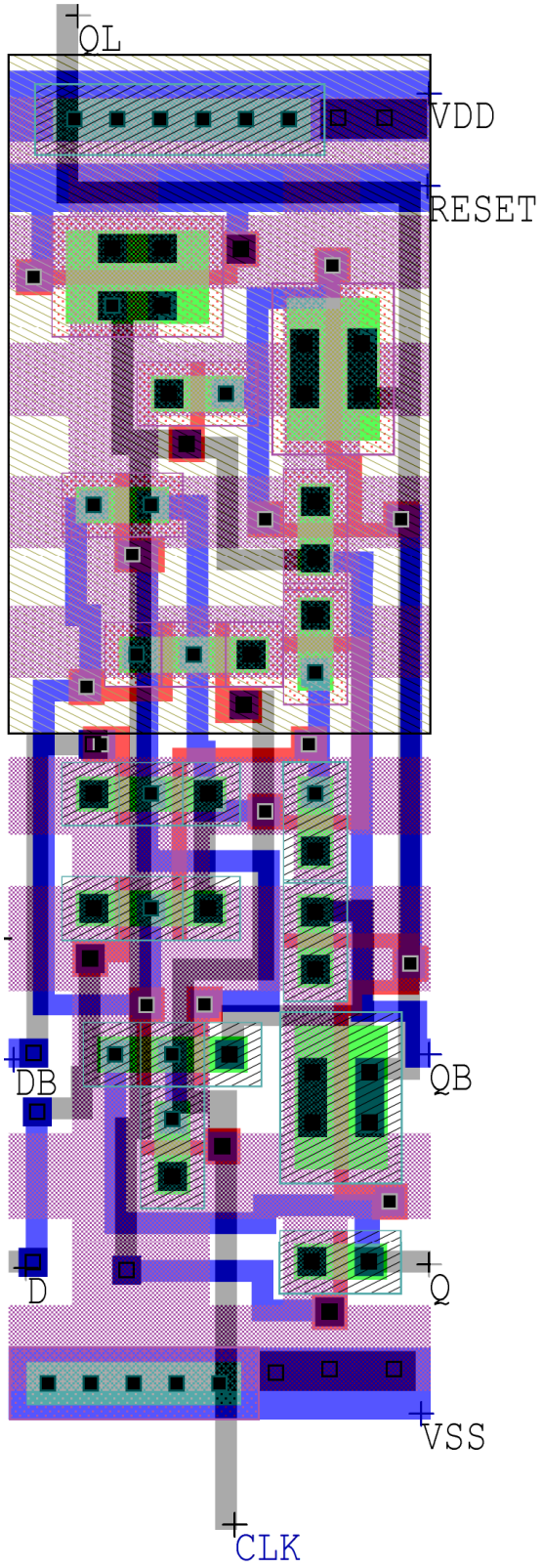

Fig. 5. Flip-Flop Layout used in LVS and DRC checks. 19 transistors total with sizing of 0.6μm and 2.4μm

additional layout. We ran into a problem with the bottom left corner of the chip and had to change the placement of some of the flip flops. This is why some of the flip flops are laid out sideways along the bottom and the side.

We equally contributed to the project since we mostly worked on the project as a group. We estimate that 200 man hours were spent on the project. The number of hours is so great due to the fact that our first design failed. The first design was based on dynamic logic and couldn't run at the slow clock speed needed for row select. We had to start from scratch to produce a new design capable of static operation.

Name	Hours
Walter Gordy	60
Josh Kotobi	60
Miguel Gallegos	60

Fig. 6. Total hours worked per person.

References

[1] J.Yuan and C.Svensson, "New Single-clock CMOS Latches and Flip-flops with Improved Speed and Power Savings," IEEE JSSC, vol. 32, pp. 563-573, Apr. 1997. pp. 62-69

[2] T. Yalcin, N. Ismailoglu, "Design of a Fully-Static Differential Low-Power CMOS Flip-Flop,' IEEE Journal of Solid-State Circuits, 1999, IEEE Xplore, Feb 12, 2012

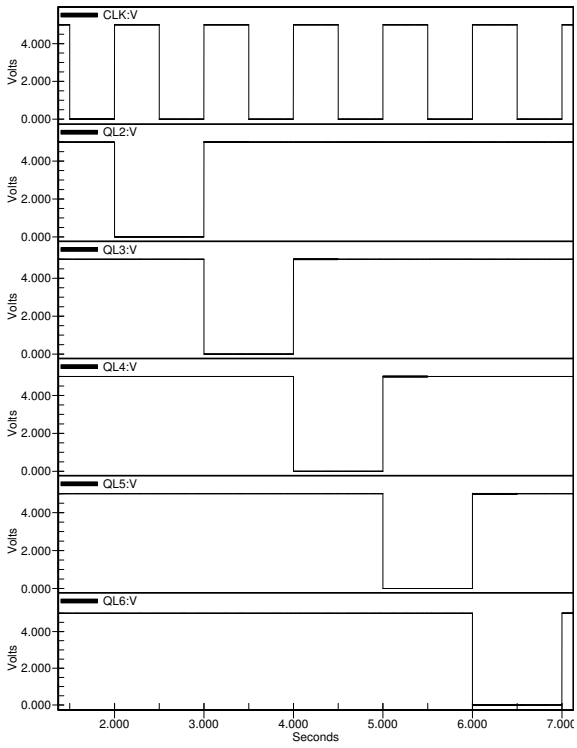

Fig. 7. Functionality of flip-flop at 1Hz, showing static operation.

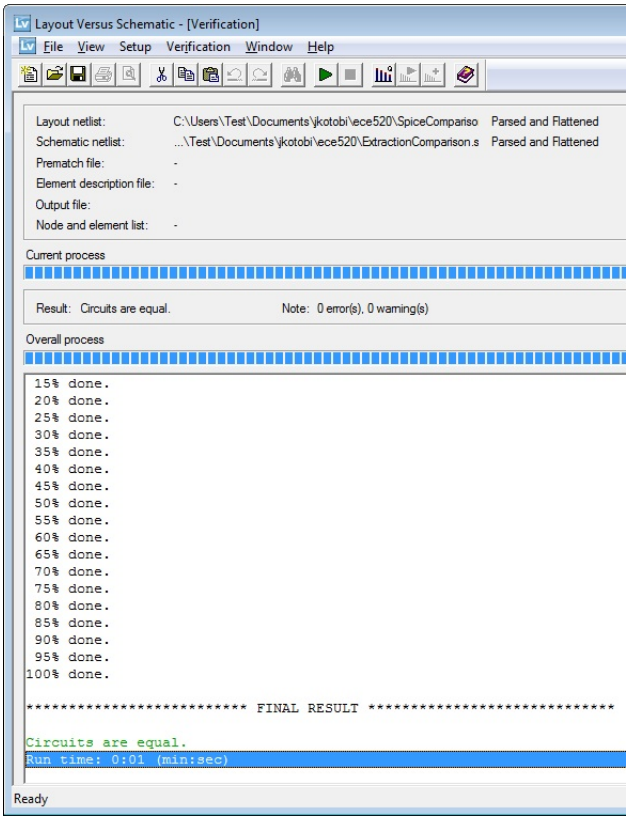

Fig. 9. LVS screen capture showing that the transistor layout is the same as the spice file

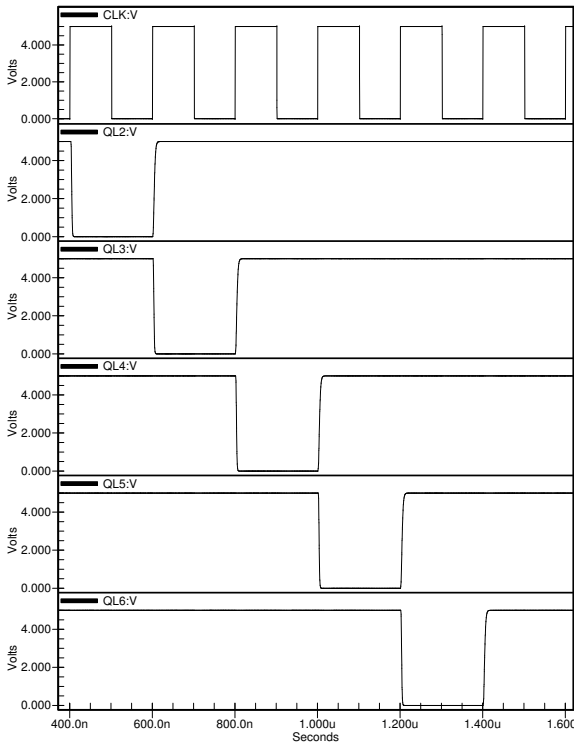

Fig. 8. Functionality of flip-flop at 5Mhz, showing maximum clock rate.

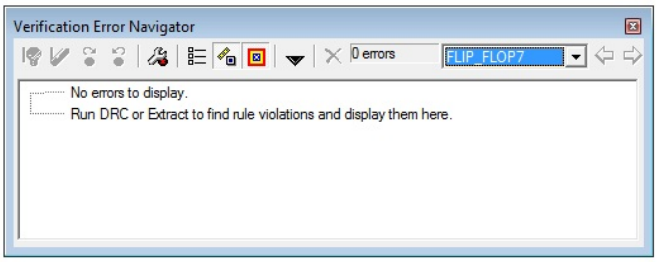

Fig. 10. DRC screen capture showing that the transistor layout passes the design rules check