

Design of Fully-Static Low-Power CVSL CMOS 128-Bit Shift Register

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Abstract—The design proposed is a 128-bit shift register, created from CVSL CMOS technology. The shift register is designed and simulated using t-spice to optimize area, speed, and robustness. The shift register proposed will be used in a 128x128 pixel CMOS camera fabricated in 0.6μm technology.

I. INTRODUCTION

THE project will consist of two phases. In the first phase, the schematic of the project will be discussed and the functionality is verified using SPICE simulations. The second phase, to come later, will discuss the layout of the shift register on silicon. Many different design implementations were tried, and we concluded that the CVSL flip flop proposed by Yuan and Scensson was best suited for our technology.

II. SOLUTION METHODOLOGY

We began our investigation with the basic behavior of the flip flop simulated in VHDL. This allowed us to experiment with connecting the flip flops and verify behavior through simulation. We choose to use a D-type flip flop. The flip flops for the shift register are initially reset, and an additional flip flop is connected at the beginning of the chain with its inputs fixed. The inputs of the initialization flip flop is tied to Vdd and ground, and its outputs are switched to the first flip’s inputs. This allows us to generate a single pulse after reset which will ripple through the shift register, creating the pattern we need.

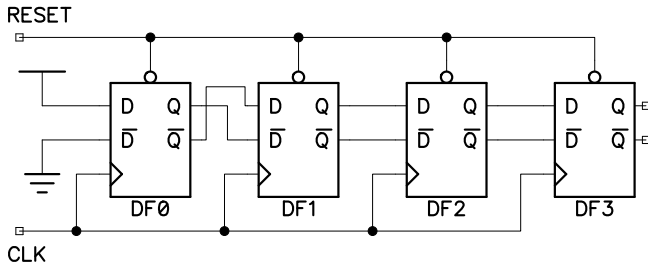


Fig. 1. Flip Flop chain showing the initialization flip flop and the first three flip flops of the shift register.

After investigating the behaviour of the flip flop, we tried several different flip-flop designs. We concluded that the most robust design would be a Differential CVSL CMOS flip-flop, first demonstrated by Yuan and Svensson[1]. This flip-flop has several distinct advantages. The flip flop is

differential driven and more immune to noise. It is also designed to be low power and small area. An improvement to the flip-flop was proposed by Yalcin and Ismailolu[2] and makes the design fully static. We added the reset functionality to the flip-flop and made it capable of driving a load larger load with an additional inverter.

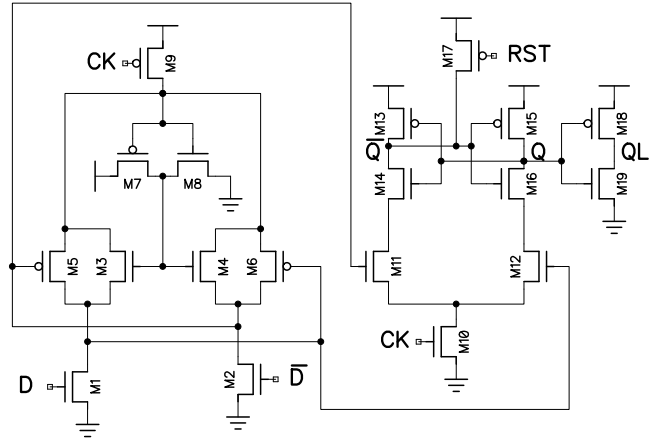


Fig. 2. Transistor Schematic of Flip Flop.

The flip flop works by utilizing two latches. While the clock is low, the slave latch holds its value and the outputs of the master latch follow its inputs. When the clock edge rises, the value of the outputs is established on the slave. Once the slave outputs are established, the outputs are held until the next rising edge. The flip flop utilizes differential inputs since differential signals are available and part of the overall design.

III. SIMULATION

The setup and hold times for the flip-flop were first simulated using only through the default parameters of our spice transistor model. The setup and hold times were measured to be approximately 350ps and 500ps respectively. After we verified the integrity of the design, we extracted the spice parameters of a real flip flop and re-measured the setup and hold times. With the extracted model of L=0.6μm and W=2.4μm, the setup and hold times were measured to be 1100ps and 745ps. This was a major difference, but did not affect the target performance of the design

The rise time and fall times were measured using the extracted spice model and compared to the default model. The results were so similar, so we present only the results of the more accurate extracted model. The rise time under normal capacitive load of 1.3pF is 3.49ns, and the fall

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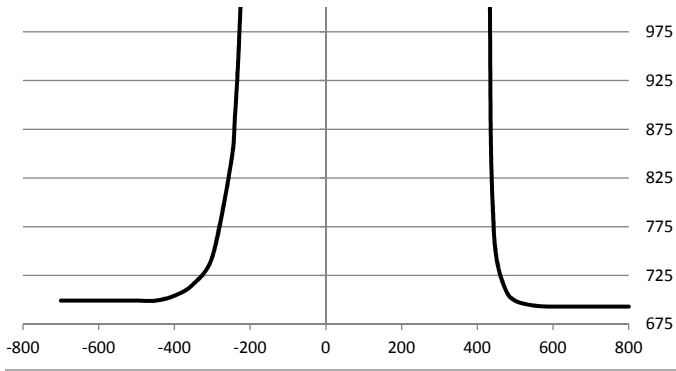


Fig. 3. Setup and Hold Times with spice model only. Axis are picoseconds

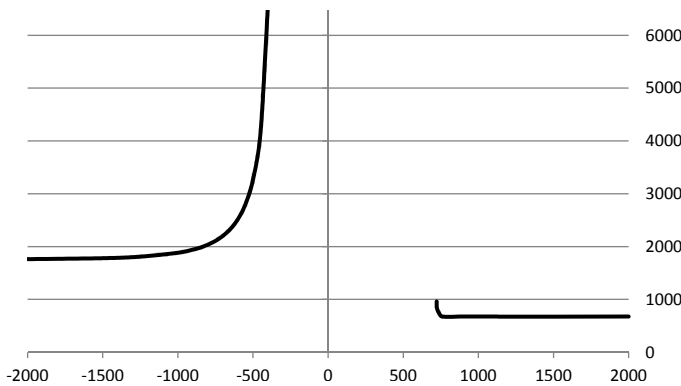


Fig. 4. Setup and Hold Times with extracted transistor capacitance. Axis are picoseconds

time is 1.70ns. This puts our design well in a safe area operation since we will clocking our design with a 200ns clock maximum (5Mhz). Additional rise and fall times were computed to verify robustness under all possible load possibilities. The flip flop was designed to drive a capacitive load of 20pF to allow us to bring the signal to an external pad if needed. The 100pF test was needed to verify functionality should the engineer need to attached a scope probe the the external pad. The scope probe was estimated to be 75pF in addition to the 20pF of the pad, this is approximated as 100pF. The design under all test situations works well within the design constraints.

	1pF	1.3pF	10pF	20pF	100pF
Rise Time	2.75ns	3.49ns	25.8ns	51.45ns	257ns
Fall Time	1.36ns	1.70ns	11.8ns	23.0ns	117ns

Fig. 5. Rise and fall time, estimated using extracted transistor capacitance.

We ran additional performance tests to measure the minimum and maximum clock frequencies, and to verify that the design would work under all possible test conditions. The design is capable of fully static operation, and has a maximum clock frequency of 5Mhz under 100pF load, and a maximum clock frequency of 75Mhz under 1.3pF load.

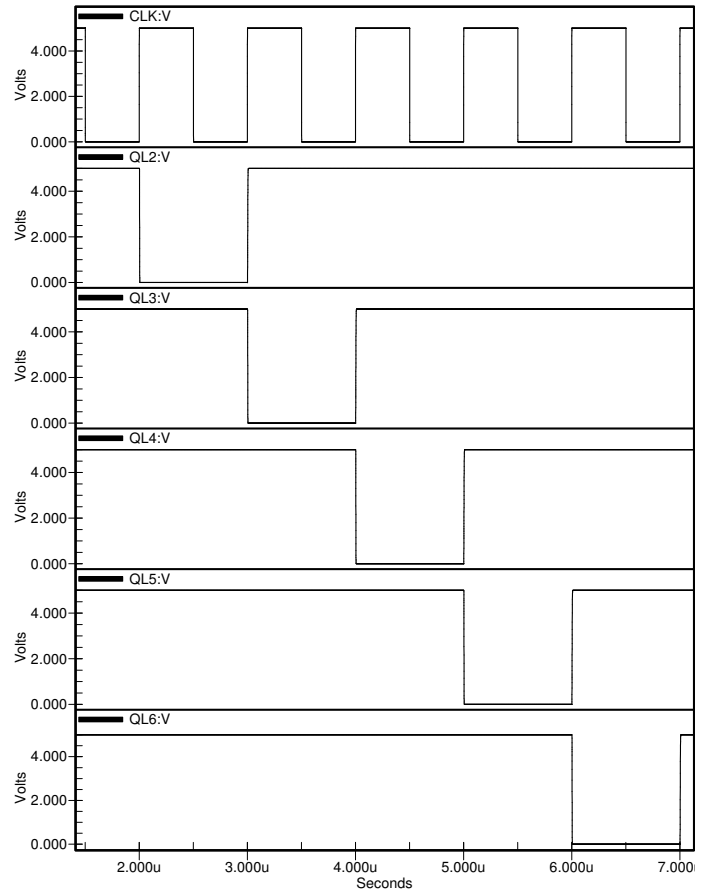


Fig. 6. Functionality of Flip Flop at 1Mhz, showing standard operation with a load capacitor of 1.3pF.

IV. CONCLUSION

The results of the flip-flop concludes with a very robust, small area, low power design. The flip-flop tests well under all specified conditions, and should fit in the area required. This flip-flop was chosen as the result of weeks of testing and was picked out of eight different flip-flop designs we tested. We decided to extract the spice model from the transistor layout to verify design functionality after the problems we had with the dynamic logic design. The transistors were laid out at with 0.6 μ m and 2.4 μ m. There are nineteen transistors in the design. Sixteen transistors are 2.4 μ m width and the other three are 9.6 μ m.

Our design was initially based on dynamic logic, and tested extremely well with a very small footprint. The design was capable of driving 2nF loads at 1Mhz, however the design failed at low frequency due to the dynamic nature of the design. At 140khz and below, the flip-flop was unable to hold the charge long enough to function properly.

REFERENCES

- [1] J.Yuan and C.Svensson, "New Single-clock CMOS Latches and Flipflops with Improved Speed and Power Savings," IEEE JSSC, vol. 32, pp. 563-573, Apr. 1997. pp. 62-69
- [2] T. Yalcin, N. Ismailoglu, "Design of a Fully-Static Differential Low-Power CMOS Flip-Flop," IEEE Journal of Solid-State Circuits, 1999, IEEE Xplore, Feb 12, 2012

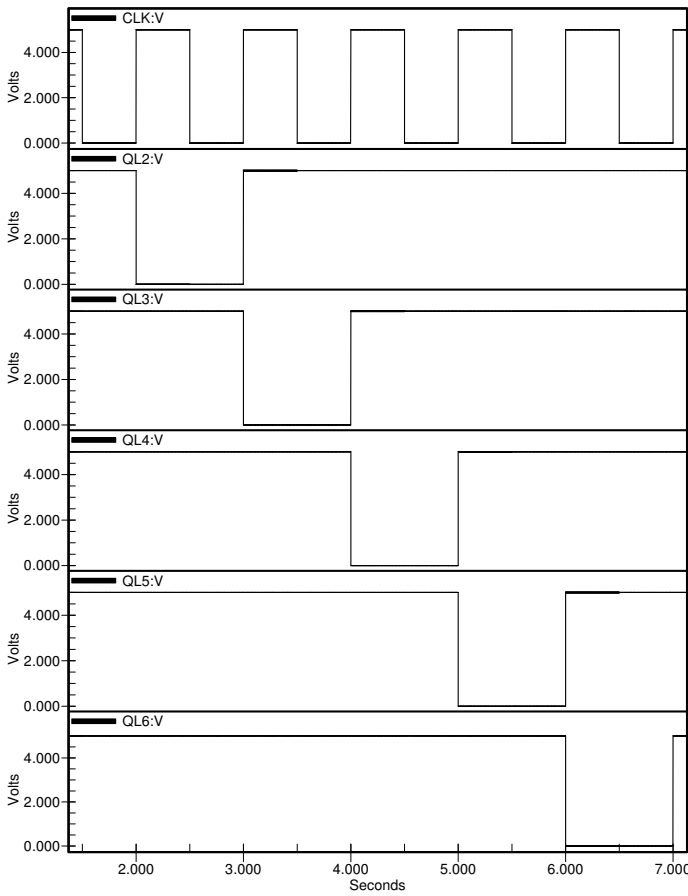


Fig. 7. Functionality of Flip Flop at 1Hz, showing static operation.

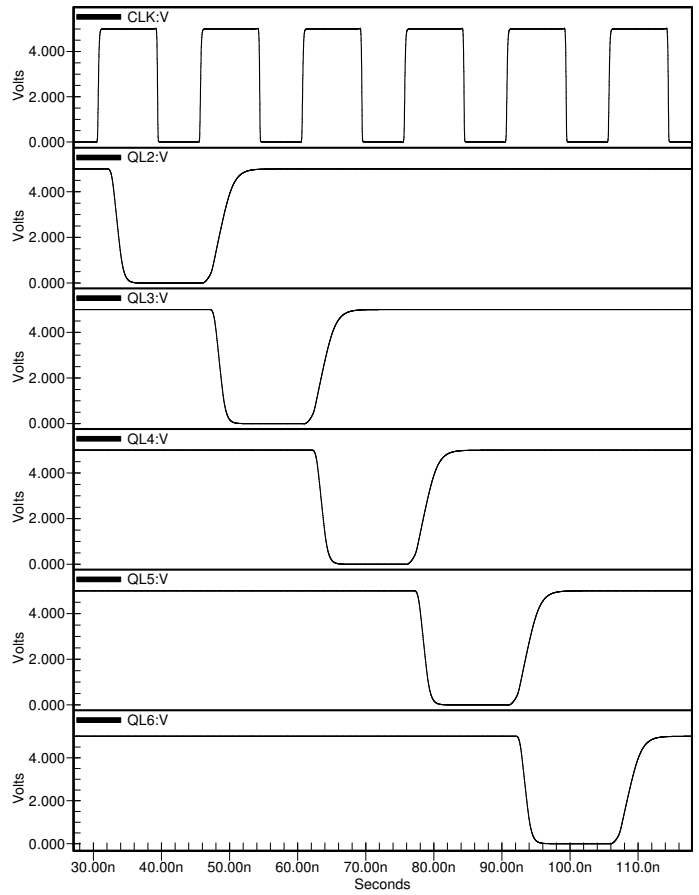


Fig. 8. Functionality of Flip Flop at 75Mhz, showing maximum operation.