Proposal for Voltage Regulator and BJT Amplifier

Walter L Gordy, Robert W Sanchez, Phillip M Mazzei, Nathan A Heermann

***Abstract*—The goal of this paper is to discuss our design methodology and review our simulation results of the final project. The project consists of two parts, designing a voltage regulator and designing a multi-stage bjt amplifier.**

I. Introduction

WE wish to manufactor high quality power supplies and bipolar junction transistor (BJT) amplifier technology. Our proposal presents two designs, one for a 120V AC to 12V DC voltage regulator and one for a multistage BJT amplifier. Each of these designs are specified to meet the commercial temperature range of 10-80°C. The voltage regulator is to output a constant 12 volts with a tolerance of 1%. The amplifer is to have a voltage gain (A_v) of 40, maximum output swing of at least $\pm 0.7V$, an input resistance of $70k\Omega$, and an output resistance of 40Ω.

II. Voltage Regulator Solution Methodology

For the design of the voltage regulator, we choose to implement a circuit containing a zener diode. Our first design uses a bridge recifier, a resistor, and a zener diode, see Fig 1. The zener diode has a breakdown voltage of 12V. We expected to see a very clean voltage regulation, but we had a larger amount of ripple than we expected. In the simple voltage regulator, as the load changed, so did the regulation tolerance. For our second attempt we incorporate a transistor.

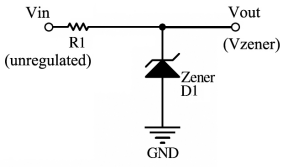

Fig. 1. Zener Voltage Regulator Circuit

To improve on this design, we included a transistor, see Fig 2. We used the transistor as an emitter follower. We choose to bias the transistor at 12.7V to get a regulated voltage of 12V, $V_{OUT} + V_{BE(ON)}$. We further improved on the design by including a low pass filter leading into the base of the transistor. This was all done in an attempt to isolate the zener diode from the load of the circuit.

With the transistor incorporated into the design, we were able to more accurately regulate the voltage keeping the ripple ≤ 0.02V. We simulated the circuit using the PSPICE engine included with Altium Designer Summer 2010. Fig 3 shows several different load values. The lowest resistive load that will stay within 1% tolerance is 300Ω. The regulator is also capable of handling no load and has a maximum value of 12.06V. When a load of 1200Ω is used, the regulation is almost 12V exactly.

Gordy, Sanchez, Mazzei, and Heermann are with the Department of Electrical Engineering, University of New Mexico, Albuquerque, NM 87106.

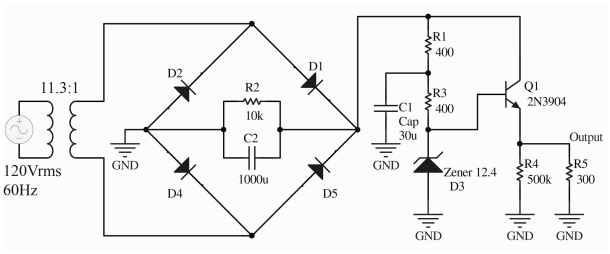

Fig. 2. Voltage Regulator Circuit

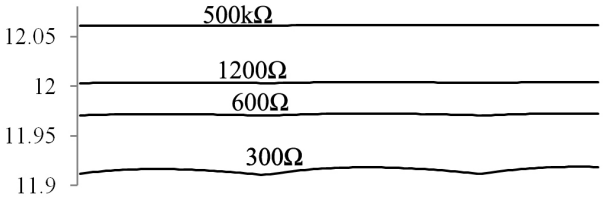

Fig. 3. Load vs Voltage Regulation

III. BJT Amplifier Solution Methodology

Our design is a simple brute force strategy. We implement three stages in our amplifer, input, gain, and output. The input stage will have an input resistance of $70k\Omega$. The gain stage will have a voltage gain of 40. The output stage will be capable of driving a 40Ω load. The entire system will be driven by a 12V power supply.

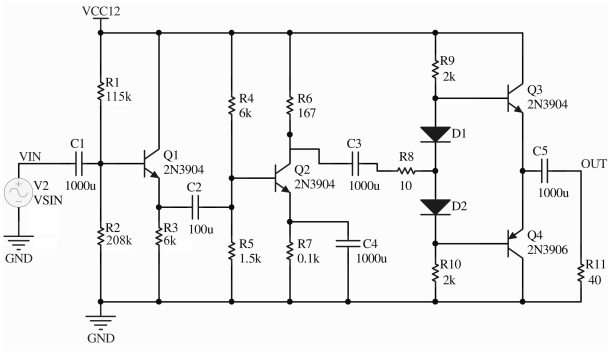

Fig. 4. BJT Amplifier Circuit

The input stage is an emitter follower. We choose the transistor to have a quiesent current of $1mA$. To approximate the Q-Point, we choose V_{CEQ} to be 6V, right in the middle of the power supply voltage. That leaves another 6V to drop across R_e.

We find R_e is similar to:

$$R_e \cong \frac{V_{CC} - V_{CEQ}}{1mA} = 6k\Omega \tag{1}$$

Now that we know R_e, we need to find R_1, R_2, and r_π. We pick R_1 and R_2 to form a voltage divider above 6V + V_{BE}. Using these three formulas we are able to find R_1, R_2, and r_π. $R_1 = 115k\Omega$, $R_2 = 208k\Omega$, $r_\pi = 5.72k\Omega$, and $\beta = 220$.

$$r_\pi = \frac{\beta V_T}{I_{CQ}} \tag{2}$$

$$7.75V = 12V \frac{R_2}{R_1 + R_2} \tag{3}$$

$$70k\Omega = R_1 \parallel R_2 \parallel [r_\pi + (1+\beta)R_E] \tag{4}$$

We will assume that the gain of the input stage is nearly 1 and is not influenced by other stages. Of course this is not true, but it can be corrected in simulation by changes to the gain stage.

The output stage consists of a PNP and a NPN transistor. The configuration of the transistors in called a push-pull follower. An NPN transistor cannot sink current and a PNP transistor cannot source current. When used together, they form a follower that can operate perfectly when driving a heavy load, such as a speaker. We included two diodes to offset the $V_{BE(ON)}$ voltage of 0.7 volts. Without the diodes, we would see a crossover distortion in the output signal. The resistors in the output stage give enough current to be bring the diodes into forward conduction and provide enough current to the base of the transistors.

The gain stage's role is simply to provide voltage gain, and we choose to use a common-emitter amplifier. We had to pick a starting place, we choose to bias the transistor with 1mA of current and R_E was choosen to be 100Ω. This places V_E at 1.2V. We choose to provide 2.4 volts at the base to allow for maximum swing while keeping V_{BE} above 0.7V. This solution allows us to calculate the value of R_C alone to provide gain. We use the following equations to calculate R_1, R_2 and R_c for the emitter follower. We'll assume that R_L is a free variable that we can adjust in the output stage.

$$R_{TH} = R_1 \parallel R_2 \tag{5}$$

$$V_{TH} = V_{CC} \frac{R_2}{R_1 + R_2} = 2.4V \tag{6}$$

$$I_{CQ} = \frac{\beta(V_{TH} - V_{BE(ON)})}{R_{TH} + (1+\beta)R_E} = 12mA \tag{7}$$

$$A_v = 2g_m(R_C \parallel R_L) = 40 \tag{8}$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.012mA}{0.026V} = 462mA/V \tag{9}$$

$$r_\pi = \beta \frac{V_T}{I_{CQ}} = 477\Omega \tag{10}$$

We find $R_1 = 6k\Omega$, $R_2 = 1.5k\Omega$ and $R_C = 160\Omega$. This will give us a large voltage swing over V_{CEQ} of about 8.88V. This swing is large enough to allow us to have at least $\pm 0.7V$ swing. When we place all the stages together, we will find that the gain is no longer 40. This is acceptable since the gain should be near 40 and we can optimize our solution using simulation tools. For AC and DC analysis models see Fig 5 and Fig 6. The slope of the load lines in Fig 7 can be found with Equations (11) and (12). We find that our Q-Point is set at I_{CQ} = 15.45mA and V_{CE} = 7.87V.

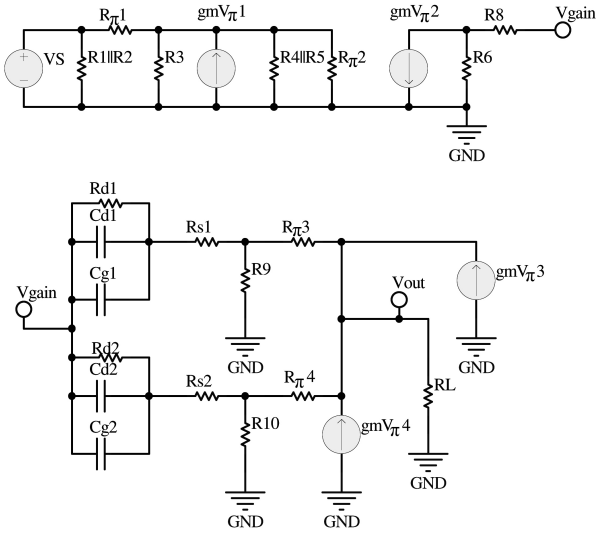

Fig. 5. AC Equivalent Circuit of BJT Amplifier

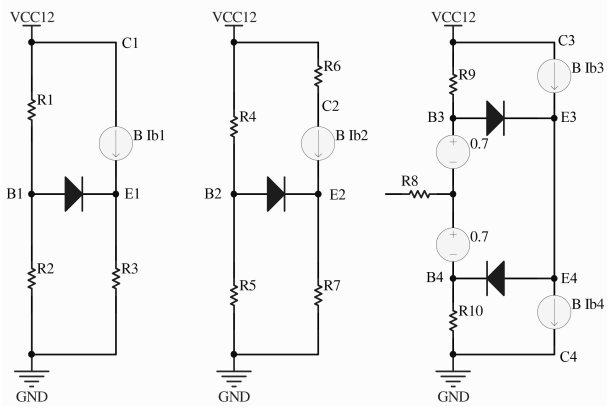

Fig. 6. DC Equivalent Circuit of BJT Amplifier

$$I_{CQ} = \frac{V_{CC} - V_{CE}}{R_C + R_E(\frac{1}{\beta} + 1)} \tag{11}$$

$$i_c = \frac{-V_{CE}}{R_C} \tag{12}$$

For schematic capture and simulation we used Altium Designer Summer 2010. Altium Designer provides an easy

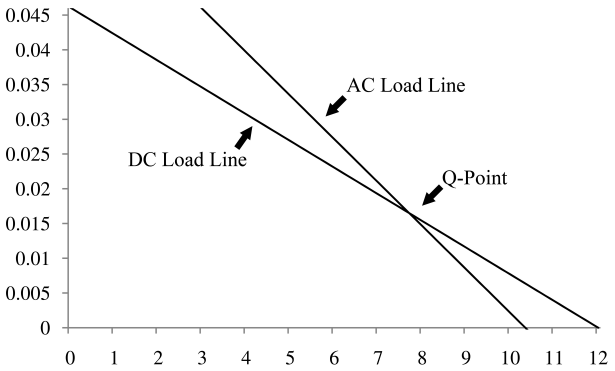

Fig. 7. AC and DC Load Lines

to use interface for editing and a powerful toolset for analyzing the circuit. We were able to use Altium's tools to do AC small signal analysis over a large frequency range and scan many parameter such as temperature and resistance. For the pspice analysis, we obtained accurate pspice models from the transistors from Fairchild Semiconductor[1]. The models are included in Fig 8 and Fig 9.

```
.model 2N3904   NPN(Is=6.734f Xti=3 Eg=1.11 Vaf=74.03
+ Bf=416.4 Ne=1.259 Ise=6.734f Ikf=66.78m Xtb=1.5
+ Br=.7371 Nc=2 Isc=0 Ikr=0 Rc=1 Cjc=3.638p Mjc=.3085
+ Vjc=.75 Fc=.5 Cje=4.493p Mje=.2593 Vje=.75
+ Tr=239.5n Tf=301.2p Itf=.4 Vtf=4 Xtf=2 Rb=10)
* Fairchild pid=23 case=TO92
* 88-09-08 bam creation
```

Fig. 8. PSPICE Model of NPN BJT used in simulations.

```
.model 2n3906  PNP(Is=455.9E-18 Xti=3 Eg=1.11
+ Vaf=33.6 Bf=204.7 Ise=7.558f Ne=1.536 Ikf=.3287
+ Nk=.9957 Xtb=1.5 Var=100 Br=3.72 Isc=529.3E-18
+ Nc=15.51 Ikr=11.1 Rc=.8508 Cjc=10.13p Mjc=.6993
+ Vjc=1.006 Fc=.5 Cje=10.39p Mje=.6931 Vje=.9937
+ Tr=10n Tf=181.2p Itf=4.881m Xtf=.7939 Vtf=10
+ Rb=10)
* Fairchild  pid=66   case=TO92
* 11/19/2001 calccb update
```

Fig. 9. PSPICE Model of PNP BJT used in simulations.

Using the tools Altium provides we optimized our circuit to have a voltage gain (A_v) of 40 at 25°C. Altium provides small signal AC analysis tools and we were able to graph frequency response over a wide spectrum. In Fig 10, we see that gain increases as the temperature decreases, and gain decreases as temperature increases. In Fig 12, we see that gain decreases as the load (R_L) increases. If the load is below 10Ω we start to notice strong distortion in the output signal. When the load is 40Ω the gain is 40. Each simulation shows a stable gain in the frequency range $1kHz$ to $3MHz$. A DC offset is preset on the output line and is generally ≤ 0.05V.

[1] The PSPICE models are property of Fairchild Semiconductor and can be found at http://www.fairchildsemi.com

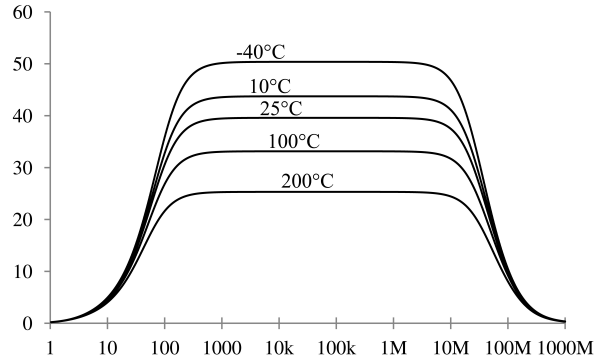

Fig. 10. Temperature and Frequency vs Gain (R_L=40Ω)

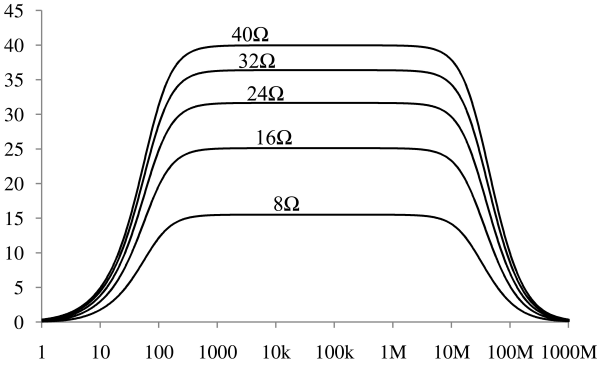

Fig. 11. Load and Frequency vs Gain (25°C)

In Fig 12 we see an example of input and output waveforms taken from simulation. The output shows a slight distortion. This is most likely caused by the capacitance in the circuit.

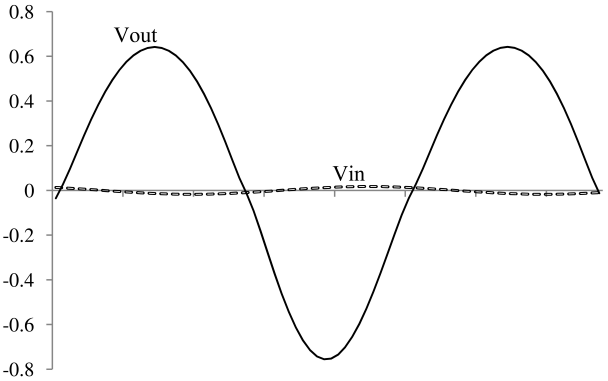

Fig. 12. 17.5mV 1kHz Input vs 700mV 1kHz Output ($A_v = 40$)

The power dissipated by the circuit was found by simulation. With a 40Ω load, the circuit has an average power dissipation of 3.86 Watts with a peak of 4.68 Watts. The input signal had an amplitude of 17.5mV and the voltage gain was 40. Little of the power dissipated is in the 40Ω resistive load consuming $210mW$ leaving about 3.65 Watts consumed by the circuit.

Parameter	Minimum	Typical	Maximum
Temperature Range	10°C	25°C	80°C
Voltage Gain	36 (80°C)	40 (40°C)	44 (10°C)
Input Resistance	-	$70k\Omega$	-
Power Dissipated	-	3.864W	4.9W
Maximum Swing	-	1V	-
Frequency Range	-	1kHz-3MHz	-
DC Offset	0	$\pm 50mV$	-

Fig. 13. Summary of Amplifier Performance

IV. Conclusion

References

[1] Donald A. Neamen, *Microelectronics, Circuit Analysis and Design*, McGraw-Hill, New York, NY, 4th edition, 2010.
[2] Paul Horowitz, Winfield Hill, *The Art of Electronics*, Cambridge University Press, New York, NY, 2nd edition, 1989.
[3] J. David Irwin, R. Mark Nelms, *Basic Engineering Circuit Analysis*, John Wiley and Sons, Hoboken, NJ, 9th edition, 2008.